In the Claims:

1. (Currently Amended) A computer system for processing instructions of a computer program, comprising:

a plurality of pipelines configured to process and execute said instructions; and

a scoreboard coupled to said pipelines, said scoreboard having a plurality of multi-bit registers, said scoreboard configured to receive a register identifier from one of said pipelines and to change a first bit in one of said multi-bit registers in response to said register identifier, said first bit indicating whether a pending write to a register identified by said register identifier exists, said register identifier associated with one of said instructions processed by said pipeline, said scoreboard further configured to ~~receive data associated with said one instruction and to change~~ control a second bit in said one register based on ~~said received data~~ whether an instruction for reading data retrieved by said pending write has been detected during said pending write.

2. (Canceled)

3. (Original) The system of claim 1, wherein said one instruction is a load instruction and said data associated with said one instruction is indicative of which memory locations have been searched in response to said one instruction.

4. (Original) The system of claim 3, further comprising circuitry configured to detect whether said one instruction can be canceled based on said second bit.

5. (Original) The system of claim 1, further comprising circuitry coupled to said scoreboard, said circuitry configured to detect a data hazard based on said first and second bits.

6. (Canceled)

7. (Canceled)

8. (Currently Amended) A method for processing instructions of a computer program, comprising the steps of:

providing a pipeline and a scoreboard, said scoreboard including a plurality of multi-bit registers;

processing one of said instructions via said pipeline;

~~transmitting a register identifier defined by said one instruction to said scoreboard;~~

~~changing a first bit in one of said multi-bit registers based on said register identifier;~~

~~transmitting data associated with said one instruction to said scoreboard;~~

~~changing a second bit in said one register based on said data; and~~

detecting that data produced via execution of said one instruction is unavailable;

detecting a pending instruction for reading said data; and

updating one of said multi-bit registers based on each of said detecting steps such that said one multi-bit register indicates an existence of a pending write associated with said one instruction and a predicate status associated with said one instruction.

~~performing said changing a first bit step in response to said step of detecting that data produced via execution of said one instruction is unavailable.~~

9. (Currently Amended) The method of claim 8, further comprising the step of detecting a data hazard based on said ~~first and second bits~~ one multi-bit register.

10. (Currently Amended) The method of claim 8, further comprising the step of indicating, via said ~~second bit~~ one multi-bit register, a speculative state of said one instruction.

11. (Canceled)

12. (Currently Amended) The method of claim 8, further comprising the steps of:

retiring said one instruction; and

transmitting a register identifier defined by said one instruction to said scoreboard,

wherein said updating step is based on ~~performing said changing a first bit step in response to~~ said retiring step.

13. (Currently Amended) The method of claim 8, ~~wherein said processing step further includes the step of executing said one instruction and said method~~ further comprising ~~includes~~ the steps of:

receiving said data ~~produced in response to said executing step~~; and

updating said one multi-bit register ~~changing said first bit~~ in response to said receiving step.

14. (Canceled)

15. (Canceled)

16. (Currently Amended) The method of claim 8, further comprising the steps of:

transmitting a register identifier defined by said one instruction to said scoreboard; and

selecting said one register based on said register identifier~~,; and~~

wherein said updating step is performed based on ~~performing said changing a first bit step in response to~~ said selecting step.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (New) The system of claim 1, further comprising circuitry configured to transmit said register identifier to said scoreboard in response to a determination that said one instruction is retired while said pending write exists.

21. (New) The system of claim 1, wherein said second bit indicates whether said pending write may be canceled, and wherein said system further comprises circuitry configured to cancel said pending write based on said second bit.

22. (New) The method of claim 8, further comprising the step of canceling a retired instruction based on said one multi-bit register.

23. (New) A system for processing instructions of a computer program, comprising:

a plurality of pipelines configured to process and execute said instructions;

a scoreboard coupled to said pipelines, said scoreboard indicative of which of a plurality of registers are associated with pending writes induced by retired instructions, said scoreboard comprising data indicative of which of said retired instructions may be canceled; and

circuitry configured to cancel at least one of said retired instructions based on said data.

24. (New) The system of claim 23, wherein said data indicates whether one of said retired instructions may be canceled based on whether a later instruction reads one of said registers associated with one of said pending writes induced by said one retired instruction.

25. (New) The system of claim 23, wherein a portion of said data is stored in a multi-bit register of said scoreboard, said data portion indicative of whether one of said plurality of registers is associated with a pending write induced by one of said retired instructions.

26. (New) The system of claim 25, wherein said data portion indicates whether said one retired instruction may be canceled based on whether a later instruction reads said one register.

27. (New) A method for processing instructions of a computer program, comprising the steps of:

processing and executing instructions via a plurality of pipelines;

updating a scoreboard such that said scoreboard indicates which of a plurality of registers are associated with pending writes induced by retired instructions;

updating said scoreboard such that said scoreboard indicates which of said retired instructions may be canceled; and

canceling at least one of said retired instructions based on said scoreboard.

28. (New) The method of claim 27, further comprising the steps of:

indicating via a multi-bit register within said scoreboard whether a pending write associated with one of said retired instructions exists and whether said one retired instruction may be canceled; and

reading said multi-bit register,

wherein said canceling step is based on said reading step.